GENARO SALAZAR RUIZ

San Diego, CA | (760) 917-4629 | gsalazarruiz@UCSD.edu | GitHub

SUMMARY

Electrical Engineer specializing in Embedded RF and Wireless Systems with 3+ years of experience in board-level design, embedded firmware, and RF validation. Skilled in full product lifecycles—from schematic capture and PCB layout to test automation and production integration. Experienced in RF synthesizers, PLLs, and VCOs up to 28 GHz for wireless and satellite systems. Proficient in optimizing signal and power integrity, low-noise design, and mixed-signal bring-up. Adept at bridging firmware and RF domains through Python-driven automation, embedded C/C++, and real-time system control.

EDUCATION

Master of Science, Wireless Embedded Systems — University of California, San Diego | Expected June 2027
Bachelor of Science, Electrical Engineering (Signal & Image Processing) — University of California, San Diego | June 2025
Associate of Science, Math & Sciences — Palomar College | June 2023
Relevant Coursework: Digital Signal Processing, Software Engineering, Digital Design, Embedded System Project, Electromagnetism

SKILLS

Hardware Design & Validation: PCB Design & Validation, Schematic Capture, Signal Integrity, Power Delivery, Crosstalk Mitigation, DFM/DFT, SoC Bring-Up, Hardware-Software Integration, Low-Power Design, Root-Cause Analysis
CAD Tools & Test Equipment: Altium, MATLAB, FPGAs (Artix-7), Oscilloscopes, Logic Analyzers, Spectrum Analyzers, JTAG/SWD, NI Test Instrumentation
Programming & Systems: C/C++, Python, SystemVerilog, ARMv8 Assembly, Linux, RTOS (Micrium OS), Bash, UART/SPI/I2C, Bootloaders, DMA

RELEVANT ENGINEERING EXPERIENCE

Z-Communications, Inc., ***Electrical Engineer (RF, Embedded Systems & Mfg. Integration)*** | San Diego, CA | Oct 2025 - Present.

- Manage ECOs, schematics, and BOM updates in Altium, coordinating with manufacturing to ensure all design changes meet DFM/DFT requirements.
- Design and test RF synthesizers and VCOs across the upper-microwave / millimeter-wave spectrum, including the so-called FR3 (approx. 7–24 GHz) band and extending through 24–28 GHz for satellite/defense applications.
- Collaborate with RF design, firmware, and manufacturing teams to perform root-cause analysis and resolve complex lock, bias, and spectral performance issues.
- Develop and maintain a Python GUI (Smart PLL Mirror) for PC-based test automation and control via UART/BLE.
- Author technician guides, assembly procedures, and troubleshooting documentation for production and sales teams.

Multiscale Ocean Dynamics, ***Electrical/Computer Engineer Aide*** | La Jolla, CA | Jan 2024 - June 2025

- Led full-lifecycle PCB development for a custom multi-MCU sonar system, from schematic capture and PCB layout to fabrication, assembly, and field deployment.
- Performed hands-on system bring-up, debugging, and validation using oscilloscopes, logic analyzers, and JTAG, identifying and correcting signal integrity and timing anomalies.
- Optimized board layout for signal integrity, crosstalk mitigation, and low-power operation in a harsh-environment, timing-critical sonar application.
- Engineered latch-based firmware to sequence MCU pings, preventing signal overlap and minimizing crosstalk in a multi-channel sonar array.
- Authored SOPs, calibration procedures, and technical documentation to ensure reproducibility and compliance.

TECHNICAL PROJECTS

Digital PLL Bare-Metal Synthesizer, *Embedded RF Engineering* Project | C / Fixed-Point DSP | Oct 2025 - Present

- Designed a microcontroller-level digital PLL from scratch using a fixed-point Q16.16 implementation, modeling the phase detector → loop filter → NCO feedback pipeline.
- Modeled Chebyshev II and Butterworth loop filters for noise vs. stability trade-offs; derived discrete PID coefficients and built firmware for lock detection and integral wind-up control.

Camera PCB & Wireless Imaging, *Embedded System Engineering* Project | C, Python, ESP32-WROOM | March 2025 - June 2025

- Designed a custom OV2640 camera PCB with an ESP32, optimizing RF PCB traces and low-power operation for reliable Wi-Fi OTA streaming.
- Developed firmware for real-time image capture and processing, implementing buffer and connection checks to prevent system crashes under poor network conditions.

Digital Design & RTL, *Hardware Engineering* Project | SystemVerilog, Artix-7 | December 2023 - September 2024

- SHA-256 Optimized SHA-256 pipeline for FPGA deployment, reducing ALUT usage from 14,000 → 1,200, improving throughput via K-map simplifications and pipeline shortcuts by 90%; integrated into a Bitcoin mining system.
- Designed ECC encoder/decoder for secure data integrity; verified with ModelSim simulations and test benches.
- Developed FSM-based UART TX/RX with synchronized states for memory-safe read/write operations; verified through waveform simulations.
- Built an LCD decoder for Sony IR remote using a 6.8 kHz timing scheme; validated with test benches and hardware verification on BASYS3 board.